Docket No YOR920030175US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Allen et al.
Case:	YOR920030175US1
Serial No.:	10/661,041
Filing Date:	September 12, 2003
Group:	2811
Examiner:	Cuong Q. Nguyen

Title: Techniques for Patterning Features in Semiconductor Devices

AFFIDAVIT UNDER 37 C.F.R.§1.131

We, the undersigned, hereby declare and state as follows:

1. We are the named inventors of the above-referenced U.S. patent application.

2. On or around November, 2000, we prepared the enclosed document (labeled "Exhibit 1") that evidences a reduction to practice of an invention falling within one or more of the claims of the above-referenced application.

3. On page 3 of the document, an image is shown (situated on the left-hand side of page 3) (hereinafter "the image") that illustrates etching through a photoresist layer (top layer), an antireflective material layer (middle layer) and a portion of a substrate layer (lower layer).

4. As is shown in the image, a critical dimension reduction occurred during etching of the antireflective material layer. This is further evidenced by the caption to the image, which indicates a -30 nanometer critical dimension bias.

5. As shown in the image, critical dimension reduction occurred during etching of the antireflective material layer, as etching is shown to have ceased just following passage through the antireflective material layer.

6. All statements made herein of our own knowledge are true, and all statements made on information and belief are believed to be true.

7. We understand that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and may jeopardize the validity of the application or any patent issuing therefrom

Date: _____ Scott D. Allen

Date: 4/8/05 Katherina E. Babich

Date: _____ Steven J. Holmes

Date: _____ Arpan P. Mahorowala

Date: 4/8/05 Dirk Pfeiffer

Date: _____ Richard Stephan Wise